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Atty. Docket No. PIA30957/DBE/US
Application No: 10/712,740

Remarks

Applicant and his representatives wish to thank Examiner Malsawma for the detailed explanations in the Office Action dated May 8, 2006 and for the courteous and helpful discussion with their undersigned representative on July 12, 2006. The claims have been amended as discussed. No new matter is introduced by the present Amendment. As discussed, the present claims are considered allowable over the cited references because one of ordinary skill would not substitute the process for depositing W (as taught by Liu) for the process for depositing Cu (as taught by Modak). Liu teaches only selective W deposition, whereas Modak teaches completely filling the dual damascene pattern with Cu. Also as discussed, Applicant submits herewith evidence that selective W deposition is a self-limiting reaction (see Wolf, *Silicon Processing for the VLSI Era*, vol. 1, 2nd ed. [2000], Lattice Press, Sunset Beach, California; p. 209, ll. 4-7). As a result, one of ordinary skill in the art would not expect selectively deposited W to completely fill a dual damascene pattern. None of the cited references teaches or discloses filling a dual damascene pattern with W, then removing some part of the W from the trench portion of the dual damascene pattern. As a result, the present claims are considered allowable over the cited references. The following remarks shall further summarize and expand upon topics discussed.

Claims 1, 2, and 7-10 have been amended. Claims 5-6 were previously canceled. New claims 12-22 have been added. Therefore, Claims 1-4 and 6-22 are active in this application.

The Rejection of Claim 1 under 35 U.S.C. § 103(a)

The rejection of Claim 1 under 35 U.S.C. § 103(a) as being unpatentable over Modak (US 6,537,913) in view of Liu (US 6,211,085) is respectfully traversed.

Modak discloses a method for making a semiconductor device with aluminum capped copper interconnect pads (Title). After filling a trench etched into the dielectric layer with copper, a portion of the copper is removed to form a recessed copper plug within the dielectric layer, and a capping layer that comprises aluminum is then formed on the recessed copper plug (Abstract and FIGS. 1a-1c).

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Liu discloses a method for forming a wolfram (W) plug within a dual damascene structure that can provide a first level metal copper contact. At the bottom of a conventional trench and hole of the damascene structure, a W film is ***selectively grown*** on the silicide. Barriers are formed on top of the wolfram and on the ***uncovered*** sides of the hole, after which copper is deposited in the remainder of the hole (Abstract; emphasis added).

One of ordinary skill would not substitute the process for depositing W (as taught by Liu) for the process for depositing Cu (as taught by Modak). Liu teaches only selective W deposition, whereas Modak teaches completely filling the dual damascene pattern with Cu. As is known in the art, selective W deposition is a self-limiting reaction (see Wolf, *Silicon Processing for the VLSI Era*, vol. 1, 2nd ed. [2000], Lattice Press, Sunset Beach, California; p. 209, ll. 4-7). For example, one cannot grow more than 10-15 nm of W by selective deposition, as the silicon necessary to selectively deposit W cannot diffuse through a W film of such thickness. Thus, one of ordinary skill in the art would not expect selectively deposited W to completely fill a dual damascene pattern.

For example, Modak discloses polishing copper layer 105 until its upper surface is separated from the surface of dielectric layer 101 by at least about 50 nanometers, and more preferably by at least about 200 nanometers (col. 4, ll. 1-4). Consequently, one of ordinary skill in the art would conclude that the dielectric layer 101 of Modak has a thickness greater than at least about 50 nanometers. Since it is known that selective W deposition cannot grow more than 10-15 nm of W, one of ordinary skill in the art would conclude selective W deposition cannot completely fill the trench 104 and via 103 in the dielectric layer 101 of Modak. As a result, one of ordinary skill in the art would not substitute the selective W deposition process of Liu with the trench-filling copper deposition process of Modak.

Therefore, the combination of Modak and Liu fails to disclose or suggest a process that completely fills a dual damascene pattern with W, then removes a part of the W from the trench portion of the dual damascene pattern (e.g., by CMP and etching, as recited in the present claim 1). Accordingly, this ground of rejection is unsustainable, and should be withdrawn.

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Claim 12 contains limitations similar to those argued above for claim 1 (notably, depositing tungsten on a first diffusion barrier to completely fill the dual damascene pattern with tungsten, and removing part of the tungsten in the trench portion so as to not expose tungsten in the contact hole portion). Claims 13-22 depend from Claim 12, and thus include all of the limitations of Claim 12. Therefore, for essentially the same reasons as Claim 1, Claims 12-22 are patentable over Modak in view of Liu.

The Rejection of Claims 2-4 under 35 U.S.C. § 103(a)

The rejection of Claims 2-4 under 35 U.S.C. § 103(a) as being unpatentable over Modak in view of Liu, and further in view of Huang (US 5,527,736) is respectfully traversed.

As explained above, the combination of Modak and Liu fails to disclose or suggest a process that completely fills a dual damascene pattern with W, then removes a part of the W from the trench portion of the dual damascene pattern. Huang fails to cure all of the deficiencies of Modak and Liu with regard to the present claims.

Huang discloses a method of metallization using a dimple-free tungsten plug. An opening is etched through an insulating layer to contact a semiconductor device structure. A layer of tungsten is deposited overlying the insulating layer and within the opening. The tungsten layer is coated with a layer of spin-on-glass that planarizes the top surface of the substrate. The spin-on-glass and tungsten layers are etched back, leaving the tungsten layer only within the opening as a tungsten plug (Abstract).

Huang appears to disclose filling only a via with W, rather than a trench and a via in a dual damascene pattern, as recited in the present claims 1 and 12. Thus, Huang cannot cure all of the deficiencies of Modak and Liu with regard to the present claims.

Furthermore, in the discussion of the background, Huang discloses an etch back process that results in recess 25 and dimple 26 (col. 1, ll. 32-34 and FIG. 2). This dimple formation ***will degrade*** the metal deposition conformity across the tungsten plug. A metal void may occur at metal level 3 or 4 if stacked via and tungsten plug methods are implemented, and the dimple may

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also increase the difficulty of intermetal dielectric planarization (col. 1, ll. 32-34 of Huang). Thus, Huang appears to teach away from a process that removes W from an opening in an insulating layer.

Therefore, the combination of Modak, Liu and Huang fails to disclose or suggest a process that completely fills a dual damascene pattern with W, then removes a part of the W from the trench portion of the dual damascene pattern, as recited in the present claims 1 and 12. Accordingly, this ground of rejection is unsustainable, and should be withdrawn.

Claims 2-4 and 7-11 depend from Claim 1, and thus include all of the limitations of Claim 1. Claims 13-22 depend from Claim 12, and thus include all of the limitations of Claim 12. Therefore, for essentially the same reasons as Claims 1 and 12, Claims 2-4, 7-11 and 13-22 are patentable over Modak in view of Liu, further in view of Huang.

The Rejection of Claims 7-8 under 35 U.S.C. § 103(a)

The rejection of Claims 7-8 under 35 U.S.C. § 103(a) as being unpatentable over Modak in view of Liu and Huang, and further in view of Chou et al. (US 2004/0005775) is respectfully traversed.

As explained above, the combination of Modak, Liu and Huang fails to disclose or suggest a process that completely fills a dual damascene pattern with W, then removes a part of the W from the trench portion of the dual damascene pattern. Chou et al. fails to cure the deficiencies of Modak, Liu and Huang with regard to the present claims.

Chou et al. discloses a method for forming an adhesion/barrier liner to improve adhesion and a specific contact resistance of semiconductor wafer metal interconnect (Abstract, ll. 1-3). Chou et al. teach that in a typical process for forming multiple layer interconnect structure, such as a damascene process, an insulating inter-metal dielectric (IMD) layer is deposited on a conductive layer, an opening is then anisotropically etched through the IMD by conventional photolithographic and etching techniques, followed by filling the opening with a metal such as tungsten, aluminum or copper. Excess metal remaining on the surface of the IMD layer may

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then be removed by a dry etchback process, for example, in the case tungsten metal is used or a chemical-mechanical polishing (CMP), for example, in the case copper metal is used. One such method known as a dual damascene technique includes the formation of a via opening in communication with an overlying trench line to form a contiguous dual damascene where both such openings are subsequently simultaneously filled with metal to form a conductive inter-layer electrical contact (via) inc communication with an intra-layer conductive line (trench line) (pg. 1, paragraph [0004]).

Chou et al. further discloses an exemplary embodiment in which, following deposition of the Ti/TiN adhesion/barrier, tungsten metal is blanket deposited onto the IMD layer 16 and into the via opening 20 therethrough to form tungsten via filling layer 24 (see, e.g., paragraphs [0023] and [0033], and FIG. 1D). Following tungsten layer deposition, a planarization process including a CMP process is carried out to remove excess tungsten and a portion of the adhesion/barrier layer 22 overlying the IMD layer above the via level (paragraph [0033] of Huang). Thus, Huang does not appear to cure all of the Modak, Liu and Huang with regard to the present claims.

Although Chou et al. suggests that the CMP process may used together with a tungsten dry etchback process (paragraph [0033]), Chou et al. is silent with regard to (i) the sequence of these two steps and (ii) the structure resulting from these two steps. Given that the disclosure is made with regard to FIG. 1D, one may reasonably presume that the structure shown in FIG. 1D is intended to result from the combination of the CMP process and a tungsten dry etchback process, and it is believed that such a structure would result from a tungsten dry etchback process, followed by the CMP process.

Therefore, the combination of Modak, Liu, Huang and Chou et al. fails to disclose or suggest a process that completely fills a dual damascene pattern with W, then removes a part of the W from the trench portion of the dual damascene pattern, as recited in the present claims 1 and 12. Accordingly, this ground of rejection is unsustainable, and should be withdrawn.

Claims 2-4 and 7-11 depend from Claim 1, and thus include all of the limitations of Claim 1. Claims 13-22 depend from Claim 12, and thus include all of the limitations of Claim

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12. Therefore, for essentially the same reasons as Claims 1 and 12, Claims 2-4, 7-11 and 13-22 are patentable over Modak in view of Liu and Huang, further in view of Chou et al.

The Rejection of Claims 9-11 under 35 U.S.C. § 103(a)

The rejection of Claims 9-11 under 35 U.S.C. § 103(a) as being unpatentable over Modak in view of Liu, Huang and Chou et al., and further in view of Yang et al. (US 6,734,559) and Yuang (US 2003/00139034) is respectfully traversed.

As explained above, the combination of Modak, Liu, Huang and Chou et al. fails to disclose or suggest a process that completely fills a dual damascene pattern with W, then removes a part of the W from the trench portion of the dual damascene pattern. Yang et al. and Yuang fail to cure the deficiencies of Modak, Liu, Huang and Chou et al. with regard to the present claims.

Yang et al. discloses a self-aligned semiconductor interconnect barrier between channels and vias, which is self-aligned and made of a metallic barrier material. A channel is conventionally formed in the semiconductor dielectric, lined with a first metallic barrier material, and filled with a conductive material. A recess is etched to a predetermined depth into the conductive material, and the second metallic barrier material is deposited and removed outside the channel. This leaves the conductive material totally enclosed in metallic barrier material. The metallic barrier material is selected from metals such as tantalum, titanium, tungsten, compounds thereof, alloys thereof, and combinations thereof (Abstract, ll. 1-3).

Yang et al. discloses a cross-section of a semiconductor wafer 200 with a (tungsten) via 210 in a dielectric (oxide) layer 212, and a recessed first channel 201 disposed in a stop (nitride) layer 214 and a first channel dielectric (oxide) layer 226 (col. 4, ll. 14-19, and FIG. 3). FIG. 3 also shows the semiconductor wafer 200 after the deposition of a barrier layer 221 and a seed layer 222 around the recessed first channel 201. The recessed first channel 201 would be formed of copper or a copper alloy. The surface of the recessed first channel 201, the barrier layer 221, and the seed layer 222 have been subject to chemical-mechanical polishing (CMP) to be level

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with the first channel dielectric (oxide) layer 226. The surface of the recessed first channel 201 has then been etched back or recessed to reduce its height by a "predetermined" thickness which is approximately the thickness of a self-aligned semiconductor interconnect barrier (col. 4, ll. 20-34). Thus, the disclosure of Yang et al. is similar to Modak (except that Yang et al. does not fill a trench ***and*** a via with copper, and is thus arguably further removed from the present claims than is Modak), but different from the present claims (which recite filling a dual damascene pattern with tungsten [W]).

Yuang discloses a dual damascene structure and method of making same (Title), in which a dielectric barrier sidewall-protected via, in combination with a conventional metal barrier, is integrated in a dual damascene process (Abstract, ll. 1-3). Yuang teaches that damascene wiring lines can be used to form bit lines in DRAM devices, with processing similar to the formation of W studs in logic and DRAM devices (paragraph [0005]), but it appears that the phrase "damascene wiring lines" in this context refers to a single damascene process.

Yuang also suggests that WN (tungsten nitride) can be used as a barrier layer 25 in a dual damascene structure 11 to isolate copper metal and avoid diffusion of copper atoms, which usually cause a leakage current. However, Yuang does not disclose or suggest that the barrier layer 25 can completely fill the dual damascene structure 11.

Yang et al. and Yuang both appear to be silent with regard to (i) completely filling a dual damascene pattern with tungsten and (ii) removing a part of a material that completely fills the dual damascene pattern from the trench portion of the dual damascene pattern. Consequently, Yang et al. and Yuang fail to cure the deficiencies of Modak, Liu, Huang, and Chou et al. with regard to the present claims.

Therefore, the combination of Modak, Liu, Huang, Chou et al., Yang et al. and Yuang fails to disclose or suggest a process that completely fills a dual damascene pattern with W, then removes a part of the W from the trench portion of the dual damascene pattern, as recited in the present claims 1 and 12. Accordingly, this ground of rejection is unsustainable, and should be withdrawn.

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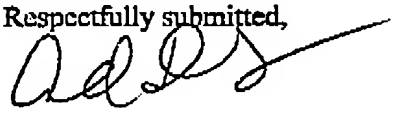
Claims 2-4 and 7-11 depend from Claim 1, and thus include all of the limitations of Claim 1. Claims 13-22 depend from Claim 12, and thus include all of the limitations of Claim 12. Therefore, for essentially the same reasons as Claims 1 and 12, Claims 2-4, 7-11 and 13-22 are patentable over Modak in view of Liu, Huang and Chou et al., further in view of Yang et al. and Yuang.

Conclusions

In view of the above amendments and remarks, all bases for objection and rejection are overcome, and the application is in condition for allowance. Early notice to that effect is earnestly requested.

If it is deemed helpful or beneficial to the efficient prosecution of the present application, the Examiner is invited to contact Applicant's undersigned representative by telephone.

Respectfully submitted,



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SILICON PROCESSING
FOR
THE VLSI ERA

VOLUME 1:
PROCESS TECHNOLOGY
Second Edition

STANLEY WOLF Ph.D.

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6.7 CVD OF METALS, SILICIDES, AND NITRIDES FOR ULSI APPLICATIONS

CVD has also been pursued as a thin-film deposition technology for a number of metals used as interconnects in ULSI, including tungsten, aluminum, titanium, and copper. Of this group, only CVD of tungsten has found wide acceptance as a production process in multilevel interconnect structures for technologies with feature sizes below 1 μm. As of 1999, CVD of the other metals has not been able to displace PVD (sputtering) as the main deposition technology. But the potential advantages of CVD (mainly with respect to step coverage and gap filling) continue to drive efforts to develop successful CVD techniques for the others. Here the recent status of the following conductor materials deposited by CVD: tungsten, tungsten silicide, and titanium nitride is discussed. The CVD of copper is covered in Chap. 15.

6.7.1 CVD of Tungsten (W)

Refractory metals (i.e., W, Ti, Mo, and Ta) have been investigated for various applications in the interconnect systems of silicon ICs.[3,78] Their resistivities are higher than those of Al and its alloys, but lower than those of the refractory metal silicides and nitrides. Of these metals, tungsten (W) ended up being adopted for several interconnect applications, although not as a stand-alone gate material nor as a global interconnect material. Instead it was selected to perform two other roles in IC interconnect systems. The most important of these is that of a *plug* (i.e., a material that can completely fill vias between aluminum films, as well as contact holes). It was chosen as a plug material because CVD-W provided better via-filling capabilities than did PVD aluminum at the time they were first implemented. That is, if contact holes and vias have minimum dimensions that exceed ~1.0 μm, they can be adequately covered with Al films. Because PVD films until recently could not completely fill contact holes and vias, such PVD-filled structures were called *non-filled-contacts* (and *-vias*). For technologies in which the minimum feature size is smaller than 1 μm the aspect ratios of contact holes and vias become so large that non-filled contact holes are no longer acceptable (due to excessive thinning of the PVD-Al films as they run down the sides of these steep and deep holes). A method to *completely fill* the contact holes was therefore sought. If it would have been possible to completely fill these holes with Al as well as was possible with CVD-W at that time, Al would have been used. But, since it was not, CVD-W prevailed, at least for several generations of technology (i.e., down to 0.18 μm). The second, somewhat lesser role of CVD-W is to serve as a local interconnect (for many of the same reasons listed above). The lower conductivity of W films compared to those of Al (or Cu), however, limits their use to short interconnect paths, and Al or Cu are retained for use as global interconnect materials. Here we describe the details of CVD-W film deposition. Note that although processes for forming CVD-W films both in selective[79] and blanket deposition[80] modes have been developed, most W applications in IC production use the latter.[78] Selective-W, while appearing to possess many advantages, has not been widely adopted. This is because problems with loss of selectivity and substrate damage have not been completely overcome. As such, we will focus mainly on the blanket-W deposition process.

CVD tungsten emerged as the most widely used of the refractory metals for interconnect applications for several reasons. First, it exhibits lower bulk resistivity than Ti or Ta, and about the same resistivity as Mo. (Note that the resistivity of tungsten films deposited by the hydrogen reduction of WF_6 is in the range of 7-12 $\mu\Omega$-cm.) Second, it exhibits high thermal stability,

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having the highest melting point of all metals (3410°C). Third, it has low stress (<$5x10^9$ dyn/cm^2), excellent conformal step coverage, and its thermal expansion coefficient closely matches that of silicon. Finally, it has excellent electromigration and corrosion resistance but none of the stoichiometry control problems that often plague silicides. Some of its disadvantages include: a) its resistivity, although 200 times lower than that of heavily-doped polysilicon, is still about twice as high as that of Al-alloy films; b) W films adhere poorly to oxides and nitrides; c) oxides form on W films when temperatures exceed 400°C (and thus care must be exercised to prevent oxidation, especially during subsequent dielectric deposition); and d) silicidation of the tungsten occurs if it is in contact with silicon and is exposed to temperatures greater than 600°C.

6.7.1.1 CVD Tungsten Chemistry: The chemical vapor deposition of tungsten is generally performed in cold-wall, low-pressure systems (an example is shown in Fig. 6-46). Although tungsten can be deposited either from WF_6 or WCl_6, tungsten hexafluoride (WF_6) is better suited as the W source gas, since it is a liquid that boils below room temperature (17°C). On the other hand, WCl_6 is a solid that melts at 275°C. The low boiling point makes WF_6 much easier to meter into process chambers in a reproducible way. The WF_6 compound is produced by the reaction between tungsten and fluorine, and after several refining steps a very pure product can be routinely obtained (99.999%). The main drawback of WF_6 is its high cost. In fact, it accounts for about 50% of the total cost of the blanket CVD-W process. The components within which the WF_6 is flowed from its container to the reaction chamber must also be heated, to prevent WF_6 condensation. Nevertheless, WF_6 is the W source typically employed in all three of the reactions used in CVD-W, namely reduction of WF_6 by: 1) silicon; 2) hydrogen; and 3) silane, since it can be reduced by all of these materials. The *silicon reduction* is given by:[78]

$$2\,WF_6\,(gas) + 3\,Si\,(solid) \rightarrow 2\,W\,(solid) + 3\,SiF_4\,(gas) \qquad (6.29)$$

This reaction is normally produced by allowing the WF_6 gas to react with regions of exposed

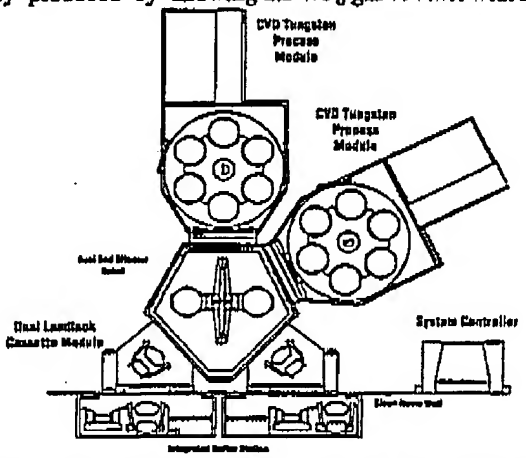

Fig. 6-46 Schematic drawing of a Novellus Concept Two CVD tungsten deposition system. Courtesy of Novellus Systems, Inc.

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solid silicon on a wafer surface at a temperature of about 300°C. The silicon surface must be quite clean (i.e., covered with less than 1 nm of native or chemical oxide) to permit initiation of the reaction. About two volumes of Si are consumed (and volatilized as SiF_4) for each volume of W formed. However, the reaction is self-limiting when the film reaches a thickness of 10–15 nm,[9,10] since the W film serves as a diffusion barrier between the Si and the WF_6 once this thickness is reached. No deposit occurs on regions of the wafer covered with SiO_2 during this reaction.

The overall *hydrogen reduction reaction* is given by:

$$WF_6\ (gas) + 3\,H_2\ (gas) \rightarrow W\ (solid) + 6\,HF\ (gas) \qquad (6.30)$$

The hydrogen reduction may result in either selective or non-selective (blanket) deposition of W. The process is carried out at reduced pressures, usually at temperatures below 450°C. Typically the process is carried out in a large excess of hydrogen. The change in the Gibbs free-energy for the reaction is -278 kcal/mole, and the film growth rate is reaction-rate limited up to a temperature of about 450°C. As noted above, the resistivity of W-films deposited by the hydrogen reduction is in the 7–12 $\mu\Omega$-cm range. The selective deposition reaction requires good nucleating surfaces. Silicon, metal, and silicide surfaces provide good sites, while SiO_2 and Si_3N_4 (especially at low temperatures), do not. On a silicon surface the deposition starts by the Si reduction, but once the W thickness becomes self-limiting, the H_2 reduction takes over. At the outset of the deposition the carrier gas used is Ar. After the Si reduces WF_6, H_2 is added to the gas flow, and the Ar flow is stopped. This deposition process is not self-limiting in thickness. A practical blanket-W process is more complex than the selective one because W does not adhere well to SiO_2. Thus, an adhesion layer is first deposited onto the SiO_2, and the W is then deposited onto it.

The overall *silane reduction reaction* is given by:

$$2\,WF_6\ (gas) + 3\,SiH_4\ (gas) \rightarrow 2\,W\ (solid) + 3\,SiF_4\ (gas) + 6\,H_2\ (gas) \qquad (6.31)$$

This reaction (LPCVD at ~300°C) is widely used to produce a W nucleation layer for the hydrogen reaction. Better nucleation is consistently obtained with the silane reduction on most surfaces, including TiN. Note that in the silane reduction, if the gas phase mixture has excess WF_6, W films are formed by the reaction, but if there is a silane excess, WSi_x films are deposited. In addition, the silane reduction of Eq. 6-31 appears to be in conflict with thermodynamic predictions. That is, the hydrogen formed in this reaction is predicted to react more readily with the WF_6 in the gas phase (to form HF) than is WF_6 to react with the SiH_4. However, experimental data indicates the reaction proceeds according to Eq. 6-31. This implies the SiH_4 reduction proceeds far from equilibrium, and the formation of HF via reaction with WF_6 is kinetically blocked (i.e., it is slow compared to the silane reaction with WF_6 to form W and SiF_4).

As noted earlier, the chemical vapor deposition (CVD) of tungsten is performed in cold-wall, low-pressure CVD (LPCVD) reactors. The wafer is held on a heated chuck opposite a showerhead through which a premixed flow of WF_6 and one of the reducing agent gases (H_2, or SiH_4) is injected. Note that hot-wall systems are not used for several reasons. First, in hot-wall systems W would also deposit on the quartz furnace-tube walls. Since W doesn't adhere to SiO_2 such films would soon delaminate from the walls and create particles. Frequent cleaning would

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